

Charge-Coupled Amplifier and Converter with Matched Offsets

Background and Summary of the Invention

5 The present invention relates to integrated image sensor circuits,
and more particularly to active integrator pixel architectures with on-
board digital converters.

Background: Active Integrator Pixel Architectures

10 The active integrator-per-pixel architecture is an effective
technique for implementing high speed, high sensitivity linear optical
arrays with analog outputs. An example of this architecture is found
in the TSL1301 102x1 Linear Sensor Array with Hold, manufactured
by Texas Instruments. (This integrated circuit and its data sheets are
all hereby incorporated by reference.) The sensor array architecture
is a key element in obtaining the desired speeds and sensitivities, and
15 has been described in detail in prior commonly owned applications:
TI-23302 - Ser.No. 09/002,731, filed January 1, 1998;
TI-23303 - Ser.No. 09/002,904, filed January 1, 1998; and
TI-24772 - Ser.No. 09/002,639, filed January 1, 1998);
all of which are hereby incorporated by reference. A feature of the
20 TSL1301 architecture is that charges representative of the integrated
photocurrent of each pixel are stored on capacitors. Current integrated
over time defines a charge, so the pixel readout signals initially appear
as a variable charge. Since this charge appears on a capacitor, it can
be read out as a voltage which is referenced to chip ground; but there

are some complications to optimally amplifying such a charge signal. Amplifiers for following such a charge signal are referred to as "charge-coupled" or charge detection amplifiers. Such amplifiers have often been used as output stages in CCD imagers, but the need for charge-coupled amplifiers extends beyond CCD imagers.

In a TSL1301 implementation, these capacitors are sequentially multiplexed into a charge-coupled output amplifier circuit so that a single serial analog output can be used to access the information from all the pixels in the array. This circuit used two inverting amplifiers so that the output increases with increasing signal. A single-supply amplifier cannot drive its output to ground quickly because the amplifier loses gain as the output nears ground.

To circumvent the output drive problem in this device, a constant offset (e.g. 100 - 200 mV typically) is introduced in the charge-coupled amplifier. This offset must either be clamped with external circuitry, or be otherwise removed in subsequent signal processing. The charge-coupled topology used in the prior art is neither effective nor efficient for driving on-board ADCs for a multiplicity of reasons. First, the offset would subtract from the dynamic range of a ground-referenced ADC. Second, a two-stage charge-coupled converter consumes more area than the disclosed invention. Finally, a two-stage charge-coupled converter is more limited with regard to settling time.

Charge-Coupled Amplifier and Converter with Matched Offsets

The present application discloses an amplifier configuration in which a single-stage inverting charge-coupled amplifier, which drives an analog-to-digital converter ("ADC"), uses the ADC's full-scale

reference as a precharge level. In some embodiments the ADC's low reference is above ground, so that the single-stage amplifier is not required to drive its output to zero volts in order to achieve a full scale range on the ADC. Thus, the innovative charge-to-voltage architecture is optimized for analog-to-digital conversion. With no charge input (corresponding to zero voltage on the sampling capacitor being converted), the one's complement output of the ADC is zero.

This architecture permits a higher throughput than the prior-art circuits, is more area efficient, and permits offset cancellation in the charge-to-voltage converters.

Brief Description of the Drawings

The disclosed inventions will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by reference, wherein:

5 **Figure 1A** shows a circuit block diagram of a preferred embodiment.

Figure 1B shows an alternative embodiment of the circuit of Figure 1A.

10 **Figure 2** shows a current product implementation of the preferred embodiment.

Figure 3 shows waveforms at selected nodes of the amplifier.

Figure 4A shows an implementation of the preferred embodiment in a scanner.

15 **Figure 4B** shows a block diagram of a sensor chip used in the scanner of Figure 4A.

Detailed Description of the Preferred Embodiments

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood that this class of
5 embodiments provides only a few examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

Preferred Embodiment

Figure 1A is a simplified block diagram of the invention. Input voltages $V_1, V_2 \dots V_n$ are the outputs of pixel integrators fixed in an array. (Linear arrays may have hundreds of pixels, and area arrays may have far more.) Capacitors $C_1, C_2, \dots C_n$ are sampling capacitors. Amplifying element A1 is a high gain, high speed operational
15 amplifier with a switched integrator feedback capacitor C_{int} . The converter reference 102 is a stable voltage reference source (e.g. a bandgap reference). The offset circuitry 104 represents a voltage source that is a fixed fraction of the converter reference voltage 102. (Making the offset 104 proportional to the reference 102 assures that the offset is controlled and tracks the reference voltage.) The ADC
20 106 digitizes the voltage V_a present at ADC input A_{in} , with a zero code representing V_a equal to V_{refLo} , and a full scale code representing V_a input equal to V_{refHi} . (Note that a simple one's complement (all bits inverted) reverses the sense of the converter. That is, a zero code can be generated with an input of V_{refHi} , and a full scale output
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can be generated with an input of V_{refLo} .) Note that by setting the V_{refLo} to a positive voltage above ground, amplifier A1 is not required to drive the output to zero volts in order to achieve a full scale range on the ADC. In operation, voltages $V_1, V_2 \dots V_n$ are typically simultaneously sampled on the corresponding capacitors $C_1, C_2 \dots C_n$ through switches $S_1, S_2, \dots S_n$. To start a conversion cycle, switch S_a is put in the upper position (V_{refHi}), switch S_c is put in the lower position to contact V_{refHi} , and switch S_b is closed. This precharges capacitor C_{int} and capacitor C_{os} to V_{refHi} . Next, in the evaluation phase, switch S_b is then opened, switch S_a is switched to the lower position to contact V_a , switch S_c is switched to the upper position to contact ground, and concurrently switch S_1 is connected to the SUM node. Assuming non-overlapping switches, the voltage V_a on the output of amplifying element A1 will settle to the voltage $V_a = V_{refHi} - (V_1 \cdot C_1 - C_{os} \cdot V_{refHi}) / C_{int}$. (By reversing the polarity of switch S_c , the opposite polarity can be achieved.) Voltage V_a is then converted by the ADC, and the digital representation of V_a is present at the digital output D_{out} . The cycle repeats using capacitor C_2 and switch S_2 , until all pixel voltages $V_1, V_2 \dots V_n$ have been converted. In addition, note that the gain from the integrator to the ADC input A_{in} can be varied globally by varying the size of the integrator capacitor C_{int} . The gain can be incrementally adjusted with trim-at-probe techniques or with other programming means.

TSL2301 Product Implementation

Figure 2 shows a current product implementation of the preferred embodiment. The innovative control technique is currently being implemented in the TSL2301 Linear Optical Sensor Array manufactured by Texas Instruments. The TSL2301 is a linear (102 x 1) 300 dpi optical sensor array with an integrated 8-bit ADC 200, and is intended for high performance scanner applications. Light energy impinging on a photodiode of a pixel of the optical array generates photocurrent, which is then integrated by active integration circuitry associated with that pixel. During the integration period, a sampling capacitor connects to the output of the active integrator through an analog switch. A multiplicity of matched capacitors provide voltages which are multiplexed through the analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity on that pixel and to the integration time. Integration, sampling, output, and reset of the integrators are controlled by the control logic 205 in response to commands input via the SDIN connection. Reading the pixels causes the sampled value of each pixel to be converted to an 8-bit digital format and output on the SDOUT pin. The ADC 200 has a high-speed sampling circuit such that the next precharge/evaluation cycle of the charge-coupled amplifier can take place during analog-to-digital conversion. The charge-coupled amplifier A1 located in the charge-to-voltage converter 202 is precharged to the ADC reference so that with no charge input (corresponding to zero voltage on the sampling capacitor being converted), the one's complement output of the converter is zero. The amplifier A1 is also autozeroed during the precharge cycle. The

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TSL2301 also comprises a 5-bit gain register and an 8-bit offset register. Voltage and current biases are provided to the array 201, the ADC 200, and the charge-to-voltage converter circuitry 202 by an bias circuit 204. Offset correction is performed in the analog domain prior to digital conversion. An offset voltage applied to the ADC and proportional to the ADC reference is used so that the driving amplifier does not have to drive to zero volts to utilize the full input range of the ADC. (Note that this offset has nothing to do with the offset digital-to-analog converter ("DAC") used to correct for offsets of V_1, V_2, \dots, V_n from the pixel electronics.) The pixel array 201 is divided into 3 zones of 34 pixels each. There is a separate offset DAC for each of the three zones for correcting dark signal levels. A programmable gain amplifier is used for convenient amplifier control. A separate gain DAC for the programmable gain amplifier is used for each of the three zones. Data communication is accomplished through a three-wire serial interface.

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Figure 4A shows an implementation of the preferred embodiment in a scanner. A piece of paper 120 containing markings 122 is being scanned by a scanner 124. The scanner 124 may be, for example, be a small scanning system comprising a single chip, a handheld scanner comprising a small number of chips, or even a larger scanner comprising a large number of chips used for larger image scanning jobs. Light energy 128 may be projected through the markings 122 on the paper, or perhaps reflected light 126 may be used to illuminate the markings 122 for detection by the sensors 130 of the scanner 124. In this particular embodiment, the scanner 124 may comprise a number of sensor chips 130 placed linearly in a single row. Other configurations may be employed where several rows of sensor chips 130 may be used

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to perform the scanning operation.

Figure 4B shows a block diagram of a sensor chip used in the scanner of Figure 4A. The chip 130 comprises, in this embodiment, a 102x1 linear array 132 of pixels 134 (P_x-y , where x = zone, y = pixel of the respective zone). The array 132 is divided into three zones of 34 pixels each. Zone 1 contains 34 pixels designated P1-1 to P1-34, Zone 2 comprises 34 pixels designated P2-1 to P2-34, and Zone 3 comprises 34 pixels designated P3-1 to P3-34. Each pixel 134 comprises a photosensor 136, a charge integrator/amplifier 138, and a sample-hold circuit 140. The chip 130 also includes additional support circuitry for controlling and processing the photo signals. The digital I/O and control circuitry 142 provides a three-wire serial interface to external communications and also control function for all on-board circuits. A charge-to-voltage converter circuit 144 receives the pixel signal and conditions the signal for the ADC 148. It also provides a programmable gain and offset capability for each pixel zone. A bias block 146 provides voltage biasing for the pixel array circuitry 132, the ADC circuitry 148, and the charge-to-converter circuitry 144.

Waveforms at Selected Nodes

Figure 3 shows waveforms at selected nodes of the amplifier. When the precharge phase begins, switch Sb is closed, switch Sa is connected to VrefHi (precharging Cint to VrefHi), and switch Sc also connects to VrefHi (precharging Cos to VrefHi). Switch S1 is connected to the input voltage V1 charging capacitor C1. During the first evaluation phase (for the first charge-coupled circuit with capacitor C1), switch Sb is opened, switch Sa is connected to the ADC input

voltage node Va, and switch Sc is connected to ground. Switch S1 is connected to the SUM node and the voltage Va settles to a value which is then digitized. The precharge and evaluation phases continue for all subsequent inputs S2...Sn.

5 Other features and details which are also contemplated for use in the preferred embodiments, but which are not necessary for practice of the claimed inventions, are disclosed in the following co-pending applications:

10 Att'y docket number TI-27352P, Ser. No. _____ - Optical Sensor Array With Zone-Programmable Gain and Offset"; and
Att'y docket number TI-27353P, Ser. No. _____ - "Addressing and Communication for Multiple-Chip Optical Sensor Arrays".

15 Both of these are commonly owned with the present application, and have effective filing dates which are simultaneous with that of the present application, and are herein incorporated by reference.

Alternative Embodiment: No Extra Switch and Capacitor

20 **Figure 1B** shows an alternative embodiment of the circuit of Figure 1A. In this embodiment, switch Sc and capacitor Cos are not used. To start a conversion cycle, switch Sa is put in the upper position, contact VrefHi, and switch Sb is closed. This precharges capacitor Cint to VrefHi. Next, switch Sb is then opened, switch Sa is switched to the lower position to contact Va, and concurrently switch S1 is connected to the SUM node. Assuming non-overlapping switches, the voltage Va on the output of amplifying element A1 will settle to the voltage $V_a = V_{refHi} - (V_1 * C_1) / C_{int}$. Voltage Va is then

input accordingly.

According to another disclosed class of innovative embodiments, there is provided: a method for converting multiple single-ended ground-referenced charge signals to a digital representation, comprising the steps of: (a.) converting an analog input to a digital output using an analog-to-digital converter which is referenced to a first voltage, and which is also connected to receive a second reference voltage; and (b.) connecting a single-stage inverting amplifier to receive charge-coupled inputs, and to amplify said charge-coupled inputs with reference to said second voltage, and to drive said analog input accordingly.

According to another disclosed class of innovative embodiments, there is provided: a method for digitizing charge-coupled inputs in an optical sensor array, comprising the steps of: (a.) connecting one or more charge-coupled inputs from an array of photosensitive elements used for sensing light energy; and (b.) amplifying said charge-coupled inputs with an amplifier circuit, said amplifier circuit consisting of, an analog-to-digital converter which uses a first voltage as a first reference to convert an analog input to a digital output, and which is also connected to receive a second reference voltage; and a single-stage inverting amplifier which is connected to receive said charge-coupled inputs, and to amplify said inputs with reference to said second voltage, and to drive said analog input accordingly.

Modifications and Variations

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and accordingly the

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scope of patented subject matter is not limited by any of the specific exemplary teachings given, but is only defined by the issued claims.

For example, within the constraints well-known to those of ordinary skill, the disclosed innovative technique is not restricted to for linear arrays, but may also be applied to area arrays.